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Grid connected three-phase multiple-pole multilevel unity power factor rectifier with reduce components count

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Abstract: This study presents a simple design and cost-effective rectifier topology based on five-level multiple-pole structure. Better efficiency and low grid current total harmonic distortion is achieved with the constant low switching frequency operation. The proposed rectifier topology consists two set of VIENNA rectifiers to form a five-level input characteristic which is known as five-level/multiple-pole multilevel unity power rectifier (5L-M^{2}UPFR). Observer techniques are designed for the proposed in-phase quantities carrier-based average current control scheme for the rectifier. Hence, unity power and input current shaping is achieved with the reduced sensor measurements. In addition to that, a proportional+resonance controller is implemented in the grid voltage observer to achieve dynamic response and better tracking under unbalanced grid condition.

1 Introduction

Multilevel converters are becoming more attractive for many industry and academia research. Most of the commercially available multilevel inverters require a bulky phase-shifted transformer with multiple-bridge rectifiers connected at the front-end side [1, 2]. However, the volume and the weight of such configuration are large and heavy. In addition, more losses are experienced in the transformer during low utilisation due to its core resistance [3, 4]. Several new transformerless multilevel rectifier topologies with low switching frequency operation have been reported in the literature. Recent developments on high incremental voltage level rectifier topologies with reduced number of components are found namely: (i) packed U cells multilevel converter (PUC) [5], (ii) reduced-part-count diode-clamped rectifier (RPC-DCR) [6] and (iii) hybrid diode-clamped and flying capacitor rectifier (DCLP-FC) [7]. The mentioned low-cost topologies have achieved good efficiency and also proven that the filter size can be drastically reduced even with the low switching frequency operation.

However, each of these topologies has its limitations and disadvantages. For instance, a complex control algorithm is required to balance the flying capacitors of the three-phase star-configured PUC topology. While in the case of RPC-DCR topology, only two switches are reduced in each phase-leg but the total component counts are not significantly optimised. Hence, huge number of gate drivers and isolated gate supplies are still required. As for the DCLP-FC topology, a good arrangement of hybrid approach is introduced to reduce 50% of the switching devices as compared with both conventional diode-clamped and flying capacitor rectifiers. Nevertheless, a total of eight dc capacitors are still needed for this three-phase topology to synthesise a five-level phase voltage stepped waveform. Due to the involvement of dc electrolytic capacitors, the lifetime of the power converter will eventually be affected by the thermal ageing. Finally the comparison of the components count (active and passive elements) of the respective rectifier topologies is shown in Table 1.

This paper presents a new cost-effective transformerless multiple-pole multilevel unity power factor rectifier (M^{2}UPFR) as shown in Fig. 1 [8]. The proposed three-phase M^{2}UPFR utilises only six switches to synthesise a five-level input phase voltage stepped waveform, hence the component counts are greatly reduced. A low switching frequency operation with the average current control (ACC) technique is implemented for the grid current harmonic compensation. Moreover, the control algorithm is developed with observer technique. Thus, a lower cost solution is achieved with the reduction of measurement sensors needed for the feedback control loop unlike the proposed switching method presented in [8]. In addition to that, excellent dynamic response is demonstrated with the estimated performances of both grid voltage and load current during unbalanced grid condition.

2 Five-level multiple-pole unity power factor rectifier topology

2.1 Basic operating principle

A proposed five-level (5L) M^{2}UPFR topology shown in Fig. 1 is constructed using two three-level (3L) VIENNA rectifier cells in each phase-leg. The multiple-pole structure is similar to the multiple-pole multilevel diode-clamped inverter concept presented in [9]. Hence, the output terminals of both VIENNA rectifier cells are connected to the respective dc capacitors with the aid of balancing circuit as detailed in [10, 11].

Since each cell is characterised with a three-level input voltage stepped waveform, the overall performance for a five-level incremental voltage stepped is synthesised based on the switching state selection and the direction of the corresponding grid phase current stated in Table 2. Therefore, the expression for the input pole voltages of the proposed 5L-M^{2}UPFR is written as follows

$$\begin{cases} V_{am}(t) = \dfrac{V_{\rm dc}(t)}{4}\left[2 - S_{a1}(t) - S_{a2}(t)\right] \cdot \text{sign}\left(I_a(t)\right) \\ V_{bm}(t) = \dfrac{V_{\rm dc}(t)}{4}\left[2 - S_{b1}(t) - S_{b2}(t)\right] \cdot \text{sign}\left(I_b(t)\right) \\ V_{cm}(t) = \dfrac{V_{\rm dc}(t)}{4}\left[2 - S_{c1}(t) - S_{c2}(t)\right] \cdot \text{sign}\left(I_c(t)\right) \end{cases} \quad (1)$$

where $V_{\rm dc}(t)$ is the dc-link voltage and sign(.) indicates the directional flow of the respective phase current according to the condition given in (2). For simplicity, the equations in this paper expressed with phase '*a*' term are applied for the other phases '*b*'

Table 1 Evaluation comparison of the components count

Topology	Single-phase			Three-phase		
	IGBTs	Diodes	Capacitors	IGBTs	Diodes	Capacitors
5L-M^{2}UPF[b]	6	16	4	10	40	4
7L-M^{2}UPF[a,b]	7	22	5	13	58	4
7L-PUC [5]	6	6	2	–	–	–
5L-RPC-DCR[b][6]	10	16	4	22	40	4
5L-DCLP-FC [7]	4	8	4	12	24	8

[a]Components comparison between seven-level (7L) M^{2}UPF and PUC topology due to the configuration of the PUC is only able to synthesis at the minimum 7L operation
[b]Switch count include voltage balancing circuit of the series stack dc-link capacitor voltage

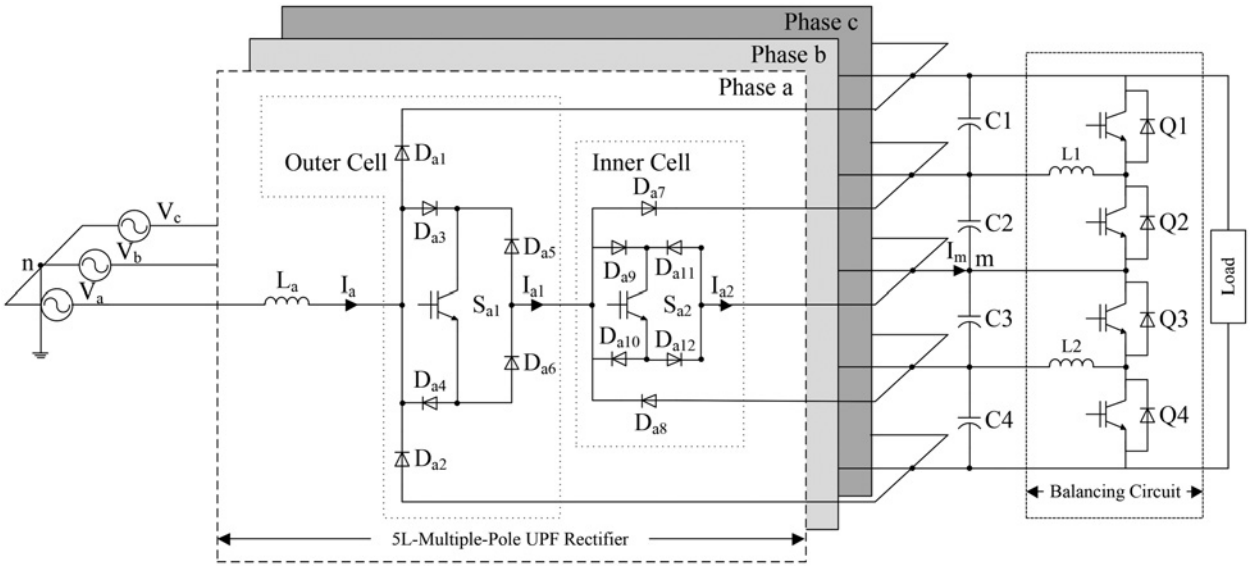

Fig. 1 *Proposed unidirectional 5L-M^{2}UPFR with the balancing circuit*

Table 2 Switching states for corresponding phase '*a*' voltage level

States	Switching		Sign(I_a)	Input pole voltage level, V_{am}
	S_{a1}	S_{a2}		
1	0	0	+	$V_{dc}/2$
2	1	0	+	$V_{dc}/4$
3	1	1	+ or –	0
4	1	0	–	$-V_{dc}/4$
5	0	0	–	$-V_{dc}/2$

Sign(I_a) is the phase '*a*' current direction flow from the grid through the switching devices

and '*c*' as well

$$\text{sign}\big(I_a(t)\big) = \begin{cases} 1 & \text{for } I_a(t) \geq 0 \\ -1 & \text{for } I_a(t) < 0 \end{cases} \tag{2}$$

The current through the four quadrant switch of the outer VIENNA rectifier cell is expressed in (3) based on the respective switching states in Table 2

$$\begin{cases} I_{a1}(t) = I_a(t) \cdot S_{a1}(t) \\ I_{b1}(t) = I_b(t) \cdot S_{b1}(t) \\ I_{c1}(t) = I_c(t) \cdot S_{c1}(t) \end{cases} \tag{3}$$

The output bidirectional current ($I_{a2}(t)$, $I_{b2}(t)$ and $I_{c2}(t)$) of the inner cell is depending on the current expression in (3) and the corresponding switching states of the inner cell switch. Hence, the neutral-point-clamped current $I_m(t)$ through node '*m*' written in (4) is the summation of these three-phase output bidirectional current

$$\begin{aligned} I_m(t) &= I_{a1}(t)S_{a2}(t) + I_{b1}(t)S_{b2}(t) + I_{c1}(t)S_{c2}(t) \\ &= I_a(t)S_{a1}(t)S_{a2}(t) + I_b(t)S_{b1}(t)S_{b2}(t) + I_c(t)S_{c1}(t)S_{c2}(t) \end{aligned} \tag{4}$$

The bidirectional current through outer and inner switches (S_{a1} and S_{a2}) of the 5L-M^{2}UPFR expressed in (5) is always positive over the fundamental period due to the floating diodes (D_{a3}–D_{a6} and D_{a9}–D_{a12})

$$\begin{cases} I_{S_{a1}}(t) = \left|I_a(t)S_{a1}(t)\right| \\ I_{S_{a2}}(t) = \left|I_a(t)S_{a1}(t)S_{a2}(t)\right| \end{cases} \tag{5}$$

The instantaneous current through the respective diode elements of both outer and inner cell are determined by the current flow over the fundamental period and expressed as follows:

Outer Cell 5L-M^{2}UPFR: During positive half cycle

$$\begin{cases} I_{D_{a1}}(t) = I_a(t)\big[1 - S_{a1}(t)\big] \\ I_{D_{a2}}(t) = 0 \\ I_{D_{a3}}(t) = I_{D_{a6}}(t) = I_a(t)S_{a1}(t) \\ I_{D_{a4}}(t) = I_{D_{a5}}(t) = 0 \end{cases} \tag{6}$$

During negative half cycle

$$\begin{cases} I_{D_{a1}}(t) = 0 \\ I_{D_{a2}}(t) = I_a(t)\left[1 - S_{a1}(t)\right] \\ I_{D_{a3}}(t) = I_{D_{a6}}(t) = 0 \\ I_{D_{a4}}(t) = I_{D_{a5}}(t) = I_a(t)S_{a1}(t) \end{cases} \tag{7}$$

Inner Cell 5L-M²UPFR: During positive half cycle

$$\begin{cases} I_{D_{a7}}(t) = I_a(t)S_{a1}(t)\left[1 - S_{a2}(t)\right] \\ I_{D_{a8}}(t) = 0 \\ I_{D_{a9}}(t) = I_{D_{a12}}(t) = I_a(t)S_{a1}(t)S_{a2}(t) \\ I_{D_{a10}}(t) = I_{D_{a11}}(t) = 0 \end{cases} \tag{8}$$

During negative half cycle

$$\begin{cases} I_{D_{a7}}(t) = 0 \\ I_{D_{a8}}(t) = I_a(t)S_{a1}(t)\left[1 - S_{a2}(t)\right] \\ I_{D_{a9}}(t) = I_{D_{a12}}(t) = 0 \\ I_{D_{a10}}(t) = I_{D_{a11}}(t) = I_a(t)S_{a1}(t)S_{a2}(t) \end{cases} \tag{9}$$

2.2 Switching function

The gating signals for the switches S_{a1} and S_{a2} based on the switching states given in Table 2 are obtained by comparing the absolute function of the modulation signal with the triangular carriers as shown in Fig. 2. The switching states are achieved according to the condition given in (10)

$$\begin{aligned} S_{a1}(t) &= \begin{cases} 1 & \text{if } M_a(t) \le V_{\text{tri1}}(t) \\ 0 & \text{otherwise} \end{cases} \\ S_{a2}(t) &= \begin{cases} 1 & \text{if } M_a(t) \le V_{\text{tri2}}(t) \\ 0 & \text{otherwise} \end{cases} \end{aligned} \tag{10}$$

where $V_{\text{tri1}}(t)$ and $V_{\text{tri2}}(t)$ are the triangular carriers and $M_a(t)$ is the phase 'a' modulation signal.

The switching function of the respective phase 'a' switches is expressed in (11), which describes the corresponding duty cycle distribution following the condition in (10) when the modulation signal crosses the edge of triangular carriers

$$\begin{cases} S_{a1}(t) = 2[1 - m\sin\omega t] \\ S_{a2}(t) = 1 - 2m\sin\omega t \end{cases} \tag{11}$$

where m is the modulation amplitude obtained according to the space vector diagram and is expressed as follows

$$m = \frac{2\sqrt{V_m^2 - \left(2\omega L P_{\text{dc}}/3V_m\right)^2}}{V_{\text{dc}}} \tag{12}$$

V_m is the amplitude of the grid voltage, L is the input line inductance, ω is the angular frequency of the grid side expressed in terms of rad/s and P_{dc} is the output power of the rectifier.

3 Device stresses for a 5L-M²UPFR topology

3.1 Voltage stress

Voltage stress analysis is essential to prevent the power devices from being damaged and affect the reliability of the converter. Thus, minimum safety requirements and smooth operations can be assured with the proper blocking capability. Two conditions are assumed for the voltage stress analysis which are: (i) negligence of overvoltage caused by the parasitic inductance due to low switching frequency operation, and (ii) negligence of transient output dc voltage caused by the inrush current since pre-charging circuit is typically employed in the dc-link for practical cases.

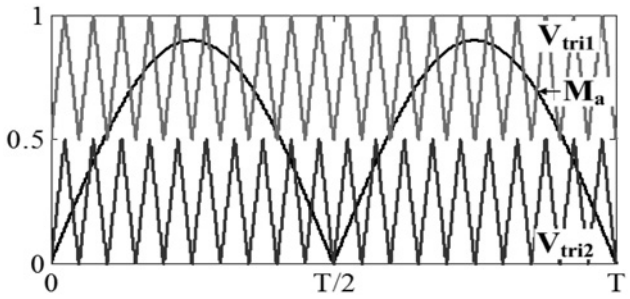

Fig. 2 *Switching scheme for 5L-M²UPFR topology*

The overall voltage stress for outer and inner cell of 5L-M²UPFR is approximately V_{dc} and $V_{\text{dc}}/2$ across the respective clamped dc-link capacitors to the negative dc rail. Therefore, the maximum voltage stress across each active component during the steady-state operation is expressed in the following equations:

Switching elements

$$\begin{cases} V_{S_{a1}} = \dfrac{5V_{\text{dc}}}{16} \\ V_{S_{a2}} = \dfrac{V_{\text{dc}}}{4} \end{cases} \tag{13}$$

Diode elements

$$\begin{cases} V_{D_{a1}} = V_{D_{a2}} = V_{\text{dc}} \\ V_{D_{a3}} = V_{D_{a4}} = V_{D_{a5}} = V_{D_{a6}} = \dfrac{5V_{\text{dc}}}{16} \\ V_{D_{a7}} = V_{D_{a8}} = \dfrac{V_{\text{dc}}}{2} \\ V_{D_{a9}} = V_{D_{a10}} = V_{D_{a11}} = V_{D_{a12}} = \dfrac{V_{\text{dc}}}{4} \end{cases} \tag{14}$$

3.2 Current stress

The maximum current stress analysis of each active component is adopted from [12] using the boundary integration of the local average pulse over one period. Several assumptions are made for the current stress analysis: (i) pure sinusoidal grid current without any ripple content, (ii) unity power factor, (iii) zero voltage dropped across the inductors, (iv) constant switching frequency, (v) balanced input grid condition and (vi) negligence of any losses in the balancing circuit. Hence, the average and root mean square (rms) of the approximated global current stress are expressed as follows

$$\begin{aligned} I_{S_{ai}\langle\text{avg}\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{\text{on}}/t_p}^{\gamma_{ai}} I_a\left(kt_p, \omega t\right)\right]\mathrm{d}\omega t \\ &\simeq \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{\gamma_{ai}t_p} I_a(\omega t)\,\mathrm{d}t_\mu\right]\mathrm{d}\omega t \end{aligned} \tag{15}$$

$$\begin{aligned} I_{S_{ai}\langle\text{rms}\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{\text{on}}/t_p}^{\gamma_{ai}} I_a^2\left(kt_p, \omega t\right)\right]\mathrm{d}\omega t} \\ &\simeq \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{\gamma_{ai}t_p} I_a^2(\omega t)\,\mathrm{d}t_\mu\right]\mathrm{d}\omega t} \end{aligned} \tag{16}$$

γ_{ai} is the switching state function of the instantaneous grid current. k is the duty cycle during turn on period. α and β are the switching times occurring at one fundamental period.

On the basis of (15) and (16), the final expression of the current stress for each switching devices is written as

$$I_{S_{a1}\langle\text{avg}\rangle} \simeq \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a(\omega t)\cdot\gamma_{a1}(\omega t)\,\mathrm{d}\omega t = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a(t)\cdot S_{a1}(t)\,\mathrm{d}t$$
$$I_{S_{a2}\langle\text{avg}\rangle} \simeq \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a(\omega t)\cdot\gamma_{a2}(\omega t)\,\mathrm{d}\omega t = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a(t)\cdot S_{a1}(t)S_{a2}(t)\,\mathrm{d}t \quad (17)$$

$$I_{S_{a1}\langle\text{rms}\rangle} \simeq \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(\omega t)\cdot\gamma_{a1}(\omega t)\,\mathrm{d}\omega t} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(t)\cdot S_{a1}(t)\,\mathrm{d}t}$$
$$I_{S_{a2}\langle\text{rms}\rangle} \simeq \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(\omega t)\cdot\gamma_{a2}(\omega t)\,\mathrm{d}\omega t} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(t)\cdot S_{a1}(t)S_{a2}(t)\,\mathrm{d}t} \quad (18)$$

Similarly, the current stress for the diode elements can also be expressed using the switching state function by extending the final current stress expressions (6)–(9) with the given switching function in (11).

4 Controller design

4.1 Unity power factor control

The proposed unity power factor control with both grid voltage and load current observers is shown in Fig. 3. The basic structure of this controller is constructed using synchronous-reference-frame (SRF) current control [13]. However, the d–q transformation in SRF control requires complicated phase lock loop design which limits the control bandwidth. Therefore, the in-phase quantities current control technique in the proposed control is implemented to eliminate the mentioned disadvantages of the d–q transformation. Moreover, two-phase operation is allowed with this proposed control which provides higher reliability in a three-phase power supply system [14].

This control method consists of dc-link voltage control at the outer loop and current control at the inner loop [9]. The outer loop control computes the dc equivalent capacitors current and regulates the output dc-link voltage. Meanwhile, the load current is formulated from the power balanced principle as shown in the following equation

$$V_{\text{dc}}I_{\text{dc}}(t) = \sum\left[V_{sn}(t) - L_s\frac{\mathrm{d}I_s(t)}{\mathrm{d}t} - R_sI_s(t)\right]I_s(t) + C_{\text{eq}}V_{\text{dc}}(t)\frac{\mathrm{d}V_{\text{dc}}(t)}{\mathrm{d}t} \quad (19)$$

The actual load current measurement is replaced with the load current control loop as shown in Fig. 4. The feed-forward observer technique is implemented to achieve better dc-link voltage tracking response during load change. The load current expression in (20) can be estimated from (19) assuming that the average power in the energy storage elements is zero

$$I_{\text{load}} = \frac{V_{\text{dc}}\left(I_{D_{a1}} + I_{D_{b1}} + I_{D_{c1}}\right)}{V_{an} + V_{bn} + V_{cn}} \quad (20)$$

V_{an}, V_{bn} and V_{cn} are the rms values of grid phase voltage. V_{dc} and I_{dc} are the mean values of the dc-link voltage and output rectifier current, respectively. Since six insulated gate bipolar transistors (IGBTs) are used in this rectifier configuration, the I_{dc} current can be easily obtained by using the feedback gating signals and the summation of the diodes current ($I_{D_{a1}}$, $I_{D_{b1}}$ and $I_{D_{c1}}$) from (6) during the positive half period.

4.2 Voltage control

To compute the equivalent dc capacitor current in the second term of (19), the dc-link voltage is regulated with a simple proportional–integral controller which is expressed as follows

$$I_{Ceq} = K_{\text{p}}\frac{\tau_i s + 1}{\tau_i s}\left[V_{\text{dc}}^*(t) - V_{\text{dc}}(t)\right] \quad (21)$$

where K_{p} is the proportional gain of the dc-link voltage regulator and τ_i is the settling time of the dc-link voltage tracking.

The approximation value of K_{p} is obtained from the energy storage model as shown in Fig. 6. The derivation of this model is

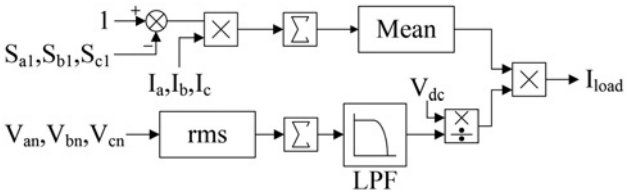

Fig. 4 *Load current observer of Fig. 3 based on presented (20)*

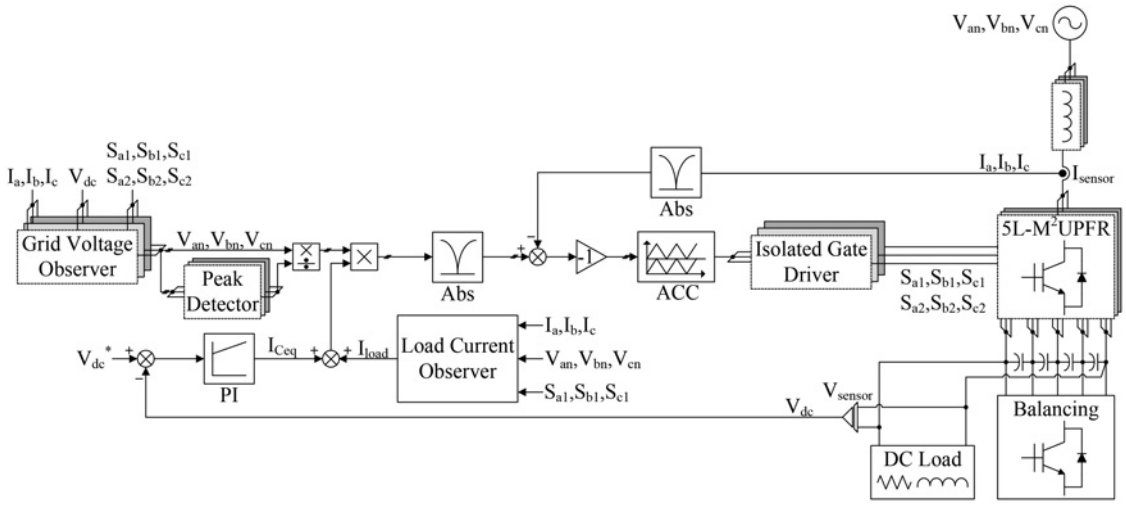

Fig. 3 *Block diagram of the unity power factor controller with the grid voltage and load current observers*

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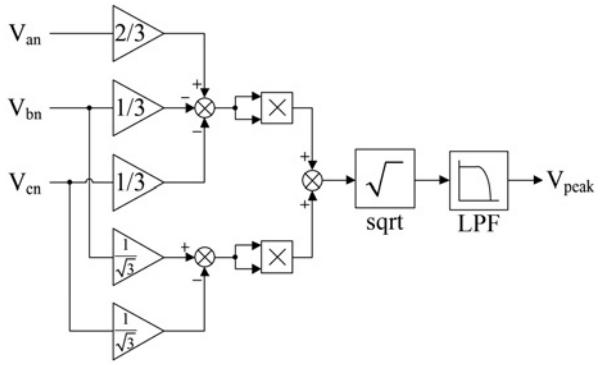

Fig. 5 *Energy storage model of the output rectifier*

based on the power balanced principle to determine the output equivalent dc capacitor current.

During the time interval from (t_0–t_1) of the charging period of the capacitors, the voltage variation due to the charge of energy storage, ΔE_{dc} is shown in the following expression

$$\Delta E_{dc} = \frac{C_{eq}}{2}\left[V_{dc}^2(t_1) - V_{dc}^2(t_0)\right] \tag{22}$$

The power of the C_{eq}, ΔP_{dc} in (23) is obtained from derivative of energy stored

$$\Delta P_{dc} = \frac{C_{eq}}{2}\frac{dV_{dc}^2(t)}{dt} = \frac{3}{2}V_m I_m - P_o(t) \tag{23}$$

where V_m and I_m are the amplitude of the grid voltage and grid current, respectively. Assuming losses are neglected for the three-phase balanced system in this case the output power and input power is equal.

According to stability criteria, the proportional gain of the control system expressed in (24) is derived from open-loop transfer function of Fig. 5 with the pole cancellation

$$K_p = \frac{3V_m\tau_i}{2V_{dc}C_{eq}P_o} \tag{24}$$

where C_{eq} is the equivalent dc-link capacitors and P_o is the average output load power.

4.3 Current control

The grid current control technique of the active rectifier can be classified into four main categories such as space vector modulation (SVM) [15, 16], fix hysteresis band current control (FHBCC) [13, 17], variable hysteresis band current control [18] and ACC [17, 19].

The SVM scheme requires high computational effort due to the complex sector control algorithm required for higher voltage stepped level rectifier topology [20]. Both HBCC and ACC can overcome the stated problems of SVM scheme. However, FHBCC scheme exhibits the disadvantage of variable switching frequency which complicates the design of the input inductance filter. The comparison performance of the FHBCC and ACC method is detailed in [17].

The carrier-based ACC scheme is applied for the proposed 5L-M^{2}UPFR and allows the desired voltage space vector to be modulated using simple analogue comparators. By doing so, lower cost implementation and lesser computational effort needed are achieved.

The input current shaping of 5L-M^{2}UPFR depends on the carrier-based modulation scheme in Fig. 2 and the condition given in (10). Hence, the current error which is the difference between the measured current and the sinusoidal reference current template will be the modulation signal $Ma(t)$ of Fig. 2.

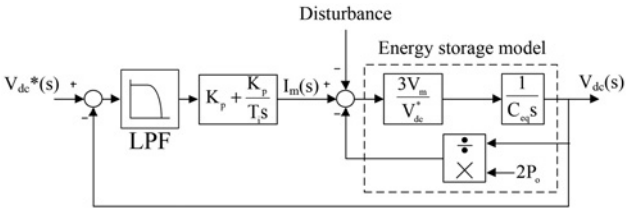

Fig. 6 *Peak detector of the grid voltage for the reference sinusoidal wave*

The sinusoidal reference current template is realised from the grid voltage and the peak detector as shown in the Fig. 3. The peak detector is designed based on the mathematical analysis of the space vector diagram as shown in Fig. 5 or this can be designed with an analogue circuit through AD633 IC.

4.4 Grid voltage observer

Several observer techniques have been proposed for various types of rectifier configuration [21–23]. Besides the advantage of eliminating the sensors needed, the observer technique reduces the size of converter and provides a lower production cost as well.

A pulse-width modulation (PWM) rectifier without voltage measurements is presented by Ohnuki *et al.* in [21]. Even though the information of three-phase grid currents are sufficient to derive and estimate the ac and dc voltages, but large dc-link voltage ripples are experienced during the computational process. Hence, causing high input current total harmonic distortion (THD) in the grid. As a result, a bulky input inductor is required to filter the current distortion.

In [22], a three-level VIENNA rectifier without current sensors is proposed. The power factor control is designed based on the phase angle difference between the grid and pole voltages of the rectifier, which is determined for calculating the modulation index space vector. Although this method provides a good dynamic response during load change, the unbalanced grid condition is not considered in this case.

The grid voltage observer of the proposed controller shown in Fig. 7 is modified from the single-phase two-stage PWM rectifier in [23]. High accuracy of grid phase voltage is estimated with three-phase grid currents and dc-link voltage measurements using the proportional+resonant control method. Low input current THD is achieved with the proposed observer and good dynamic response is performed as well for the case of one phase grid voltage down during operation.

The voltage across the input phase 'a' inductor is expressed as follows

$$\begin{aligned} V_{La}(t) + V_{Ra}(t) &= V_{an}(t) - V_{am}(t) - V_{mn}(t) \\ &= V_{an}(t) - \frac{V_{dc}(t)}{12}\begin{Bmatrix} 2\left[2 - S_{a1}(t) - S_{a2}(t)\right]\cdot \mathrm{sign}\left(I_a(t)\right) \\ -\left[2 - S_{b1}(t) - S_{b2}(t)\right]\cdot \mathrm{sign}\left(I_b(t)\right) \\ -\left[2 - S_{c1}(t) - S_{c2}(t)\right]\cdot \mathrm{sign}\left(I_c(t)\right) \end{Bmatrix} \end{aligned} \tag{25}$$

$V_{mn}(t)$ is the virtual ground voltage of node m referred to the ground terminal of node n. $V_{Ra}(t)$ is the voltage drop across the inductor core resistor of phase 'a'.

The grid phase voltage can be calculated by expanding the voltage expression in (25) and it is given by

$$\tilde{I}_a(t) = \frac{1}{L_a}\int \left\{ \begin{matrix} V_{an}(t) - R_a\tilde{I}_a(t) \\ -\frac{V_{dc}(t)}{12}\begin{Bmatrix} 2\left[2 - S_{a1}(t) - S_{a2}(t)\right]\cdot \mathrm{sign}\left(I_a(t)\right) \\ -\left[2 - S_{b1}(t) - S_{b2}(t)\right]\cdot \mathrm{sign}\left(I_b(t)\right) \\ -\left[2 - S_{c1}(t) - S_{c2}(t)\right]\cdot \mathrm{sign}\left(I_c(t)\right) \end{Bmatrix} \end{matrix} \right\} dt \tag{26}$$

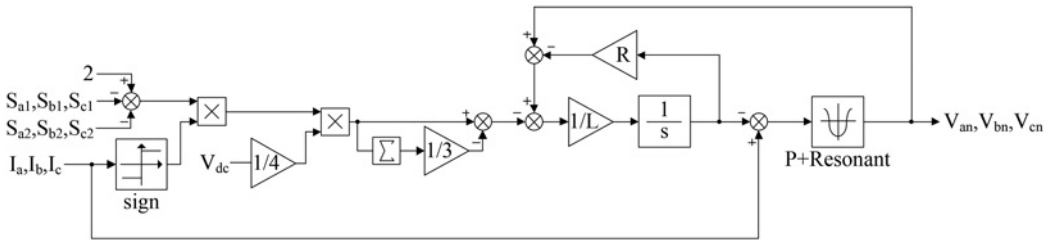

Fig. 7 *Grid voltage observer of Fig. 3 based on presented (25) and (26)*

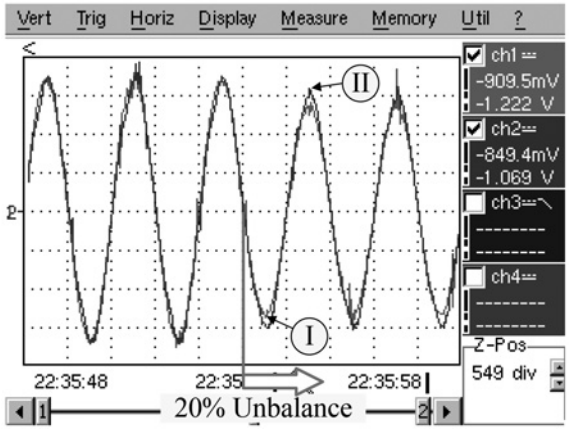

Fig. 8 *Dynamic performance of grid voltage observer comparing estimation method (I) with actual measurement (II)*

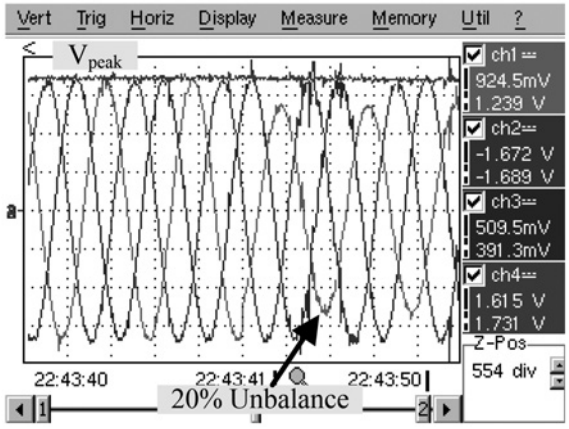

Fig. 9 *Dynamic performance of peak detector with one of the grid voltages 20% unbalanced*

From (26), a proportional+resonant controller is used for the grid phase voltage estimation and is expressed as follows

$$V_{an}(t) = \left[I_a(t) - \tilde{I}_a(t)\right] \cdot \left[K_{\mathrm{p}} + \frac{K_{\mathrm{r}} s}{s^2 + \omega^2}\right] \tag{27}$$

ω is the angular frequency of the grid side ($\omega = 314$ rad/s) and proportional gain and resonant gain is chosen to be $K_{\mathrm{p}} = 3.25$ and $K_{\mathrm{r}} = 125$, respectively.

5 Experimental results

The laboratory prototype is developed with the control algorithm implemented in the dSPACE DS1103 development controller board to verify the performance of 5L-M^{2}UPFR. Experimental

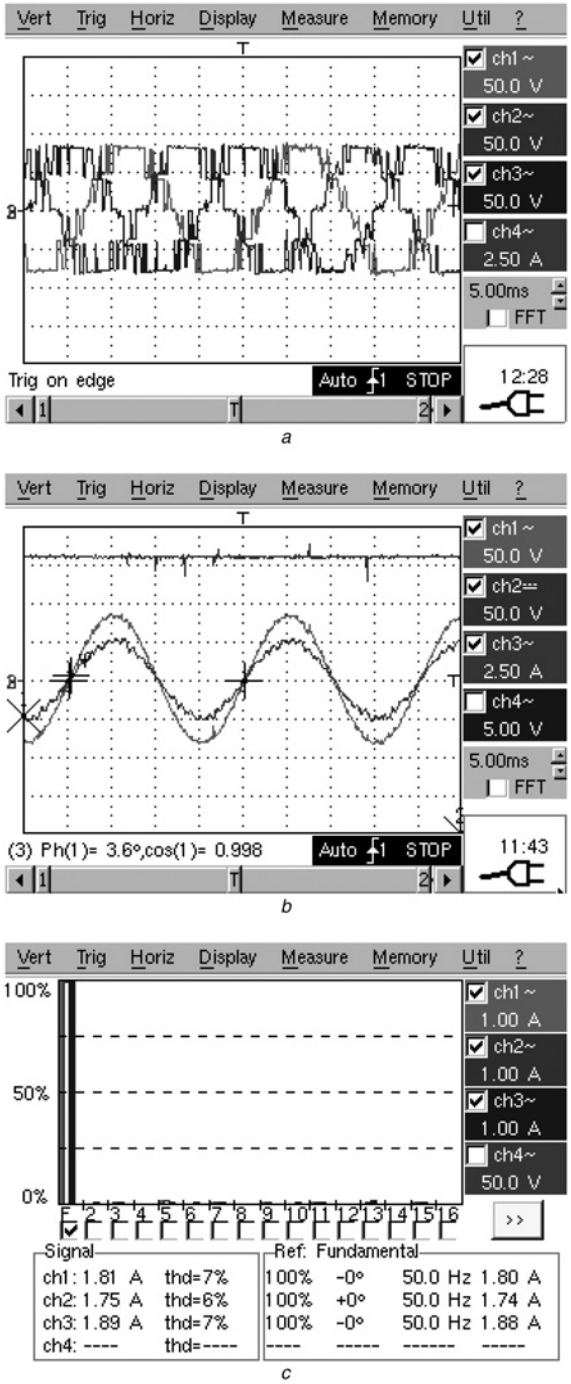

Fig. 10 *Input voltage and current performance of a 5L-M^{2}UPFR topology under balanced grid condition*

a Input pole voltage
b dc-link voltage (upper trace), grid phase voltage and line current (lower trace)
c THD of line current

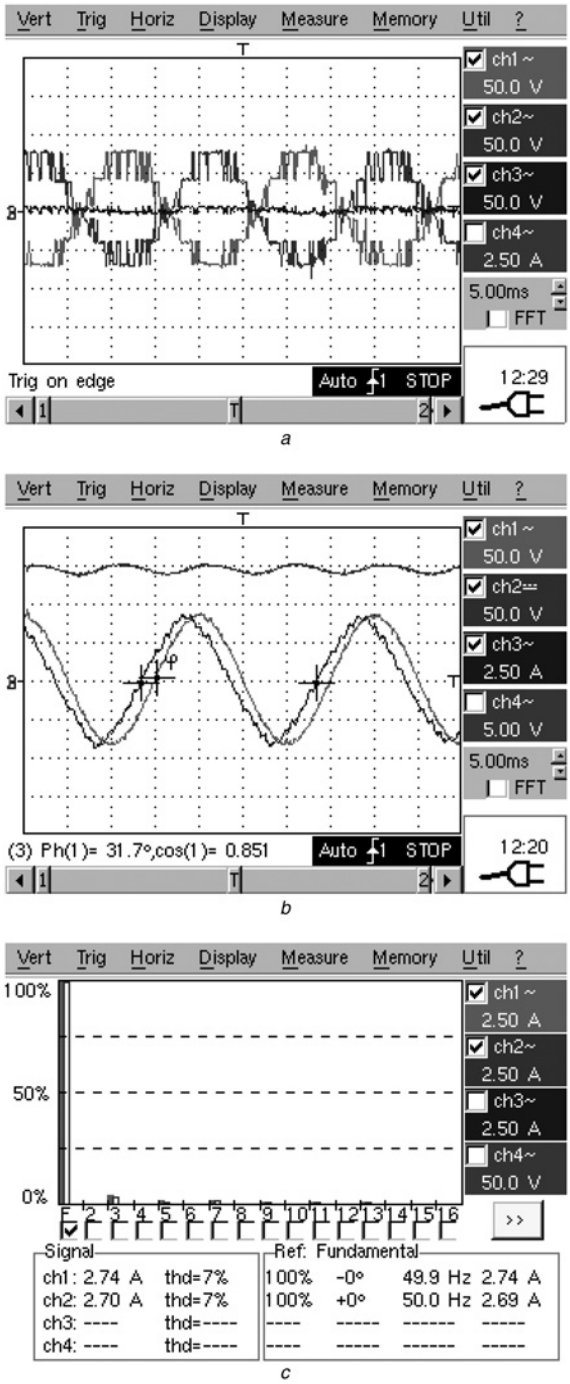

Fig. 11 *Input voltage and current performance of a 5L- M²UPFR topology under extreme unbalanced grid condition*

a Input pole voltage
b dc-link voltage (upper trace), grid phase voltage and line current (lower trace)
c THD of line current

results have proven the feasibility of the proposed 1 kHz rectifier topology with the controller based on grid phase voltage and load current observers.

The dynamic response of the grid phase voltage estimation during unbalanced grid condition is verified with both estimation and actual measurement as shown in Fig. 8. In addition to that, the peak value of the grid phase voltage obtained by the peak detector is stable in Fig. 9 even during sudden grid phase voltage changed.

The experimental results in Fig. 10 show the input characteristic performance of the new 5L-M²UPFR with the proposed controller under balanced grid supply condition. The power factor for balanced grid supply is high (PF = 0.998) and low THD current (7%) is achieved with low input inductance filter.

On top of that, the experimental results in Fig. 11 show the feasibility study of the converter response during two phase operation with the same in-phase quantity current control. Even though one of the phase voltages is down during the operation, comparatively low THD current in Fig. 11*c* is achieved with the same input inductance filter. The continuous supply under single line fault is achievable due to the proportional+resonant control loop is able to provide a fundamental angle for the sine template. This sine template is used to generate the current reference for the current loop for compensating the current distortion. By observing the system operation of the rectifier under single line fault condition, the pole voltage is seem to behave as a single phase operation with the 180° phase shifted from another pole voltage (refer to Fig. 11*a*), which reflect the line current has a slightly phase shifted from the grid phase voltage. With the supported experimental results, the proposed controller proved that high reliability of the three-phase power supply unit is achievable under extreme unbalanced grid condition.

On the bass of both experimental results obtained for balanced and unbalanced grid operation, five-level incremental stepped waveform is synthesised with the proposed low switching frequency carrier-based ACC scheme. The proposed dynamic control with the observers reduces the cost implementation and the complexity of the algorithm.

6 Conclusions

A new cost-effective 5L-M²UPFR topology is introduced in this paper to achieve high power factor and low current distortion with drastically reduced in the total number of switching devices and sensors. Moreover, isolation gate power supply is reduced since there are no complementary switches used in this proposed topology. The great advantage of this proposed rectifier is that low grid current THD is achievable with constant low switching frequency operation and the reduced input inductance filter size.

Experimental results proved the dynamic response of the proposed in-phase quantities current control using observer technique. Therefore, the proposed controller provides higher reliability of the three-phase power supply even during the extreme unbalanced grid condition. Since grid voltage and load current observers are designed in the control loop, the reduction of sensors can avoid technical issues such as sensor failure and measurement errors. On top of that, light weight and high power density can be achieved for the proposed 5L-M²UPFR.

Several technical challenges and improvements need to be considered for future development such as dc balancing and dc voltage ripple content occurred during extreme unbalance grid condition. However the dc voltage ripple can be filtered out by replacing larger filter capacitor. Thanks to the use of in-phase quantities current control using observer technique, a 0.85 power factor with current distortion of 7% during light load condition is achievable. The proposed rectifier with the control technique is recommended for high power application on ac/dcC/ac drives instead of phase-shifted transformer-based multiple-diode bridge rectifiers for energy efficiency.

7 References

1 Kouro, S., Malinowski, M., Gopakumar, K., *et al.*: 'Recent advances and industrial applications of multilevel converters', *IEEE Trans. Ind. Electron.*, 2010, **57**, pp. 2553–2580
2 Miranbeigi, M., Iman-Eini, H., Asoodar, M.: 'A new switching strategy for transformer-less back-to-back cascaded H-bridge multilevel converter', *IET Power Electron.*, 2014, **7**, pp. 1868–1877
3 Daher, S., Schmid, J., Antunes, F.L.M.: 'Multilevel inverter topologies for stand-alone PV systems', *IEEE Trans. Ind. Electron.*, 2008, **55**, pp. 2703–2712
4 Steimer, P.K., Winkelnkemper, M.: 'Transformerless multi-level converter based medium voltage drives'. 2011 IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 3435–3441
5 Ounejjar, Y., Al-Haddad, K., Grégoire, L.A., *et al.*: 'Packed U cells multilevel converter topology: theoretical study and experimental validation', *IEEE Trans. Ind. Electron.*, 2011, **58**, pp. 1294–1306

6 Corzine, K.A., Baker, J.R.: 'Reduced-parts-count multilevel rectifiers', *IEEE Trans. Ind. Electron.*, 2002, **49**, pp. 766–774
7 Itoh, J.I., Noge, Y., Adachi, T.: 'A novel five-level three-phase PWM rectifier with reduced switch count', *IEEE Trans. Power Electron.*, 2011, **26**, pp. 2221–2228
8 Gabriel, O.H.P., Maswood, A.I., Ziyou, L., *et al*.: 'Input current shaping of five-level multiple-pole VIENNA rectifier topologies with reduced component and better performance'. Presented at the 39th Annual Conf. of the IEEE Industrial Electronics Society, IECON 2013–, 2013
9 Ooi, G.H.P., Maswood, A.I., Ziyou, L.: 'Five-level multiple-pole PWM AC-AC converters with reduced components count', *IEEE Trans. Ind. Electron.*, 2015, **62**, pp. 4739–4748
10 Hatti, N., Kondo, Y., Akagi, H.: 'Five-level diode-clamped PWM converters connected back-to-back for motor drives', *IEEE Trans. Ind. Appl.*, 2008, **44**, pp. 1268–1276
11 Ajami, A., Shokri, H., Mokhberdoran, A.: 'Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter', *IET Power Electron.*, 2014, **7**, pp. 503–514
12 Kolar, J.W., Drofenik, U., Zach, F.C.: 'Current handling capability of the neutral point of a three-phase/switch/level boost-type PWM (VIENNA) rectifier'. Power Electronics Specialists Conf., 1996. PESC '96 Record, 27th Annual IEEE, 1996, vol. 2, pp. 1329–1336
13 Maswood, A.I., Fangrui, L.: 'A unity-power-factor converter using the synchronous-reference-frame-based hysteresis current control', *IEEE Trans. Ind. Appl.*, 2007, **43**, pp. 593–599
14 Minibock, J., Kolar, J.W.: 'Novel concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers', *IEEE Trans. Ind. Electron.*, 2005, **52**, pp. 162–170
15 Barbi, I., Batista, F.A.B.: 'Space vector modulation for two-level unidirectional PWM rectifiers', *IEEE Trans. Power Electron.*, 2010, **25**, pp. 178–187
16 Raj, P.H., Maswood, A.I., Ooi, G.H.P., *et al*.: 'Voltage balancing technique in a space vector modulated 5-level multiple-pole multilevel diode clamped inverter', *IET Power Electron.*, 2015, **8**, pp. 1263–1272
17 Maswood, A.I., Al-Ammar, E., Liu, F.: 'Average and hysteresis current-controlled three-phase three-level unity power factor rectifier operation and performance', *IET Power Electron.*, 2011, **4**, pp. 752–758
18 Fangrui, L., Maswood, A.I.: 'A novel variable hysteresis band current control of three-phase three-level unity PF rectifier with constant switching frequency', *IEEE Trans. Power Electron.*, 2006, **21**, pp. 1727–1734
19 Jong-Won, S., Bo-Hyung, C.: 'Digitally implemented average current-mode control in discontinuous conduction mode PFC rectifier', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 3363–3373
20 Ide, P., Froehleke, N., Grotstollen, H.: 'Investigation of low cost control schemes for a selected 3-level switched mode rectifier'. Ninteeth Int. Telecommunications Energy Conf., 1997. INTELEC 97, 1997, pp. 413–418
21 Ohnuki, T., Miyashita, O., Lataire, P., *et al*.: 'Control of a three-phase PWM rectifier using estimated AC-side and DC-side voltages', *IEEE Trans. Power Electron.*, 1999, **14**, pp. 222–226
22 Wang, B., Venkataramanan, G., Bendre, A.: 'Unity power factor control for three-phase three-level rectifiers without current sensors', *IEEE Trans. Ind. Appl.*, 2007, **43**, pp. 1341–1348
23 Ghosh, R., Narayanan, G.: 'Generalized feed forward control of single-phase PWM rectifiers using disturbance observers', *IEEE Trans. Ind. Electron.*, 2007, **54**, pp. 984–993